Tiny Package, High Efficiency, Step-up DC/DC Converter

General Description

The SL9266 is a compact, high efficiency, and low voltage step-up DC/DC converter with an Adaptive Current Mode PWM control loop, includes an error amplifier, ramp generator, comparator, switch pass element and driver in which providing a stable and high efficient operation over a wide range of load currents. It operates in stable waveforms without external compensation.

The low start-up input voltage below 1V makes SL9266 suitable for 1 to 4 battery cells applications of providing up to 300mA output current. The 450kHz high switching rate minimized the size of external components. Besides, the 17μA low quiescent current together with high efficiency maintains long battery lifetime.

The output voltage is set with two external resistors. Both internal 2A switch and driver for driving external power devices (NMOS or NPN) are provided.

Ordering Information

SL9266 □□

Package Type
E : SOT-26
X5 : SOT-89-5

Operating Temperature Range
C : Commercial Standard
P : Pb Free with Commercial Standard

Features

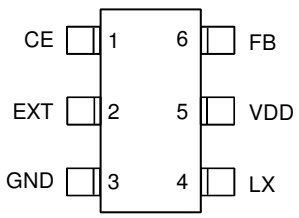
- **1.0V Low Start-up Input Voltage**
- **High Supply Capability to Deliver 3.3V 100mA with 1 Alkaline Cell**
- **17μA Quiescent (Switch-off) Supply Current**
- **Zero Shutdown Mode Supply Current**
- **90% Efficiency**
- **450kHz Fixed Switching Frequency**
- **Providing Flexibility for Using Internal and External Power Switches**
- **Small SOT-26 & SOT89-5 Package**

Applications

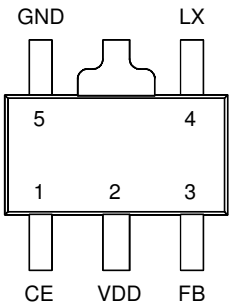
- PDA
- DSC
- LCD Panel
- RF-Tags
- MP3
- Portable Instrument
- Wireless Equipment

Pin Configurations

(TOP VIEW)



SOT-26



SOT-89-5

Typical Application Circuit

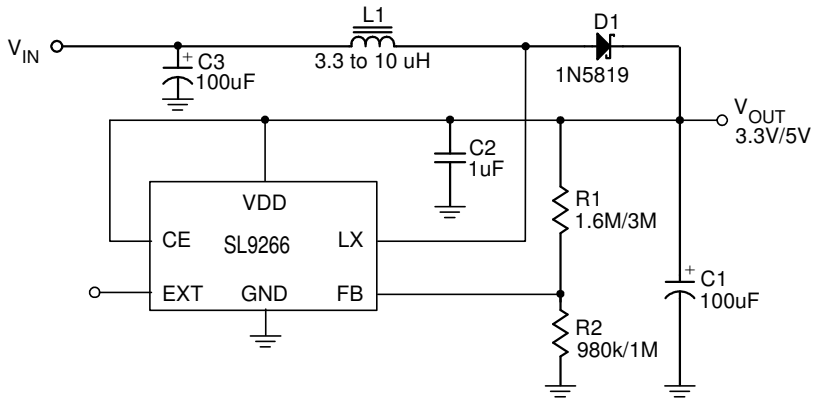


Figure 1. SL9266 Typical Application for Portable Instruments

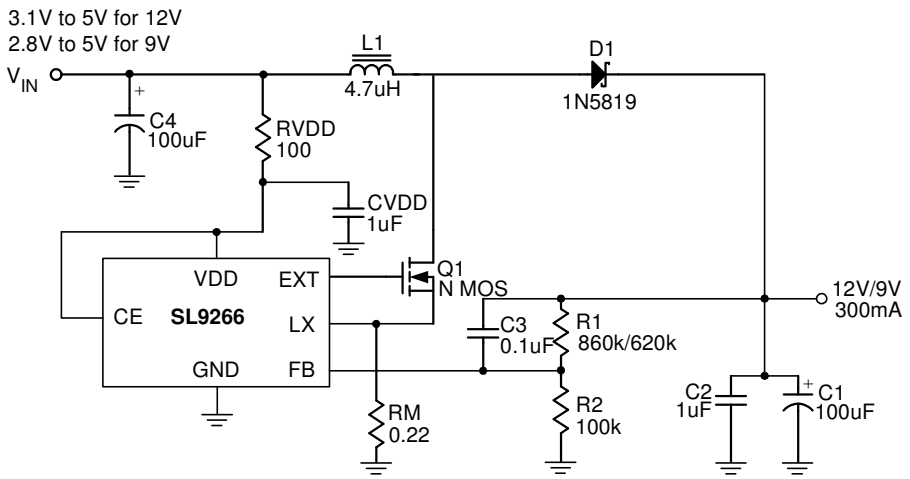


Figure 2. **SL9266** High Voltage Applications

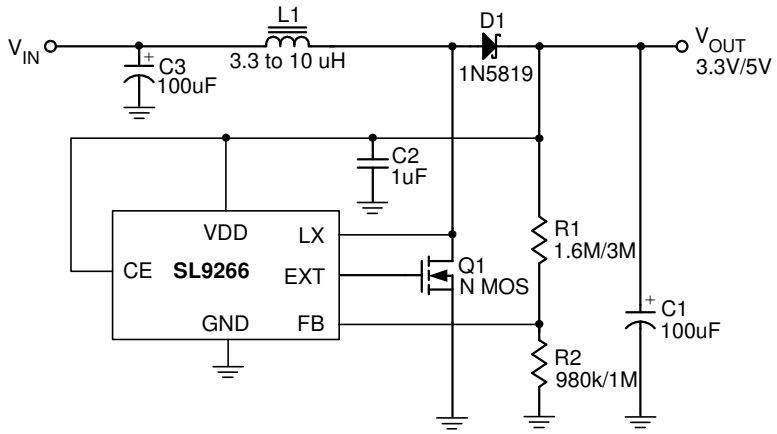


Figure 3. SL9266 for Higher Current Applications

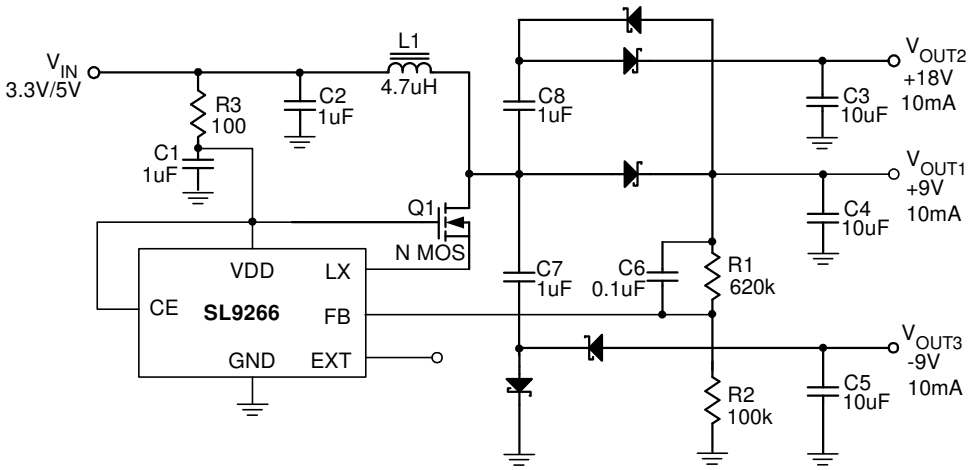
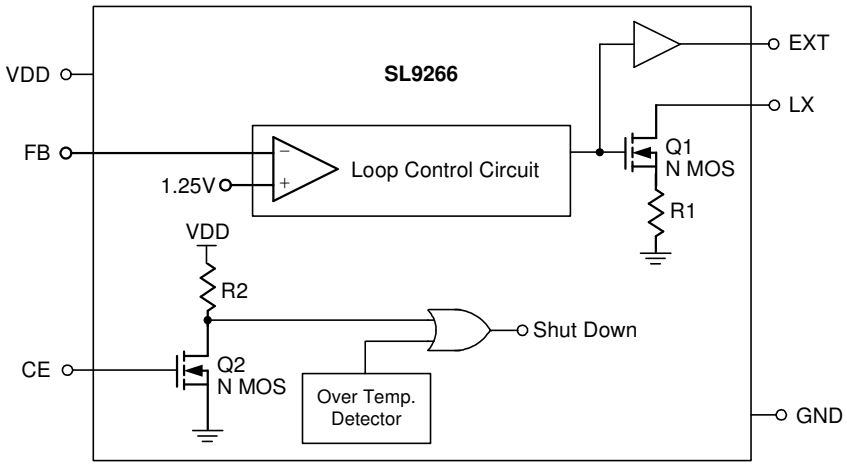


Figure 4. SL9266 for Multi-Output Applications

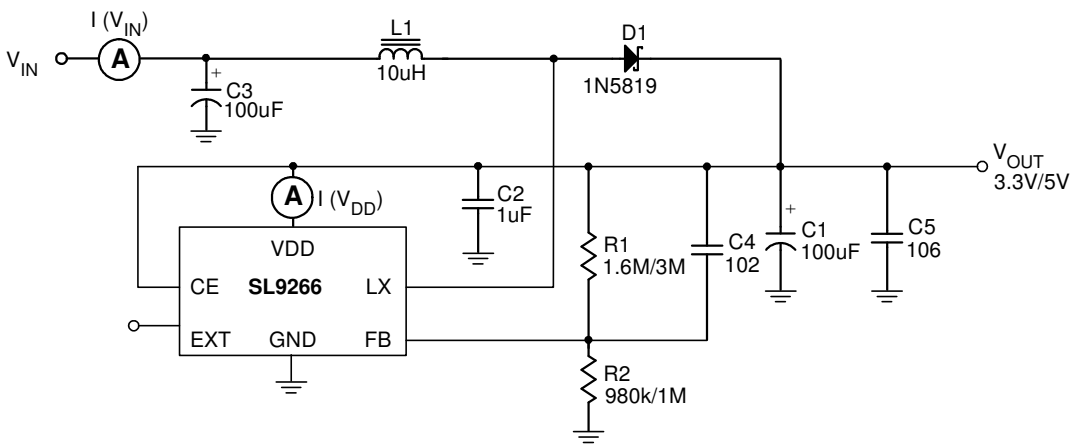
Functional Pin Description

Pin No.		Pin Name	Pin Function
SL9266CX5	SL9266CE		
1	1	CE	Chip enable SL9266 gets into shutdown mode when CE pin set to low.
--	2	EXT	Output pin for driving external NMOS
5	3	GND	Ground
4	4	LX	Pin for switching
2	5	VDD	Input positive power pin of SL9266
3	6	FB	Feedback input pin Internal reference voltage for the error amplifier is 1.25V.

Function Block Diagram



Test Circuit



Absolute Maximum Ratings

- Supply Voltage ---------- –0.3V to 7V
- LX Pin Switch Voltage ---------- –0.3V to 7V
- Other I/O Pin Voltages ---------- –0.3V to (VDD + 0.3V)
- LX Pin Switch Current ---------- 2.5A
- EXT Pin Driver Current ---------- 200mA
- Package Thermal Resistance
  SOT-26, θ_{JC} ---------- 145 °C/W
  SOT-89-5, θ_{JC} ---------- 45 °C/W
- Operating Junction Temperature ---------- 125 °C
- Storage Temperature Range ---------- –65° C to +150° C

NOTE:
Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits

Electrical Characteristics

(V_{IN} = 1.5V, VDD set to 3.3V, Load Current = 0, T_A = 25° C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Start-UP Voltage	V_{ST}	I_L = 1mA	--	0.98	1.05	V
Operating VDD Range	V_{DD}	V_{DD} pin voltage	2	--	6	V
Shutdown Current I (V_{IN})	I_{OFF}	CE Pin = 0V, V_{IN} = 4.5V	--	0.01	1	μA
Switch-off Current I (VDD)	$I_{SWITCH\ OFF}$	V_{IN} = 6V	--	17	25	μA
Continuous Switching Current	I_{SWITCH}	V_{IN} = CE= 3.3V, V_{FB} = GND	0.4	0.55	0.7	mA
No Load Current I (V_{IN})	$I_{NO\ LOAD}$	V_{IN} = 1.5V, V_{OUT} = 3.3V	--	75*	--	μA
Feedback Reference Voltage	V_{REF}	Close Loop, VDD = 3.3V	1.225	1.25	1.275	V
Switching Frequency	F_S	V_{DD} = 3.3V	425	500	575	kHz
Maximum Duty	D_{MAX}	V_{DD} = 3.3V	85	95	--	%
LX ON Resistance		V_{DD} = 3.3V	--	0.3	1.1	Ω
Current Limit Setting	I_{LIMIT}	V_{DD} = 3.3V	1.6	2	2.6**	A
EXT ON Resistance to VDD		V_{DD} = 3.3V	--	5	8.5	Ω
EXT ON Resistance to GND		V_{DD} = 3.3V	--	5	8.5	Ω
Line Regulation	ΔV_{LINE}	V_{IN} = 3.5 ~ 6V, I_L = 1mA	--	1.5	10	mV/V
Load Regulation	ΔV_{LOAD}	V_{IN} = 2.5V, I_L = 1 ~ 100mA	--	0.25***	--	mV/mA
CE Pin Trip Level		V_{DD} = 3.3V	0.4	0.8	1.2	V
Temperature Stability for Vout	T_S		--	50	--	ppm/°C
Thermal Shutdown Hysterises	ΔT_{SD}		--	10	--	°C

Note :

* No Load Current is highly dependent on practical system design and component selection that cannot be covered by production testing. Typical No Load Current is verified by typical application circuit with recommended components. No Load Current performance is guaranteed by Switch Off Current and Continuous Switching Current.

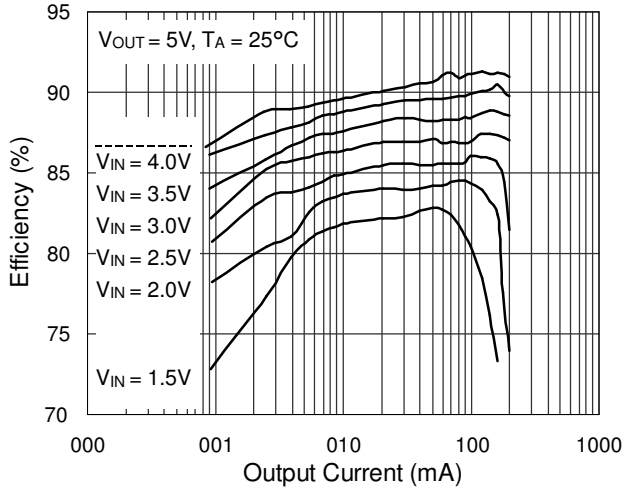
** Current Limit is guaranteed by design at T_A = 25°C.

***Load Regulation is not tested at production due to practical instrument limitation. Load Regulation performance is dominantly dependent on DC loop gain and LX ON Resistance that are guaranteed by "Line Regulation" and "LX ON Resistance" tests in production.

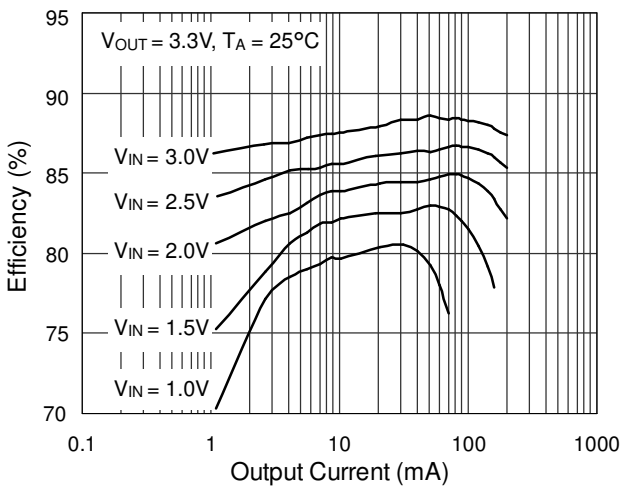
Typical Operating Characteristics

(Refer to Test Circuit)

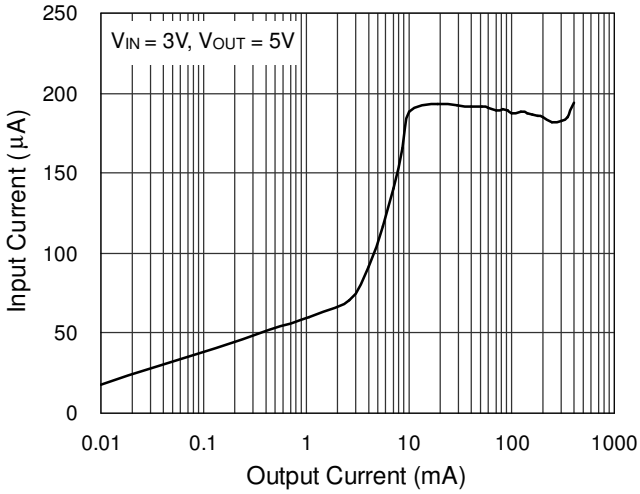
Efficiency vs. Output Current



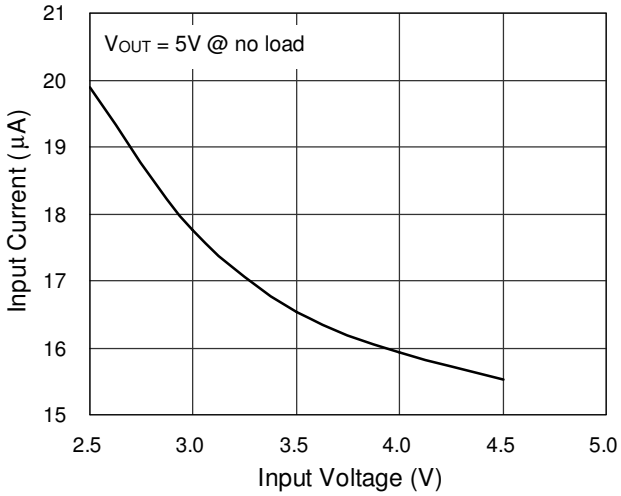
Efficiency vs. Output Current



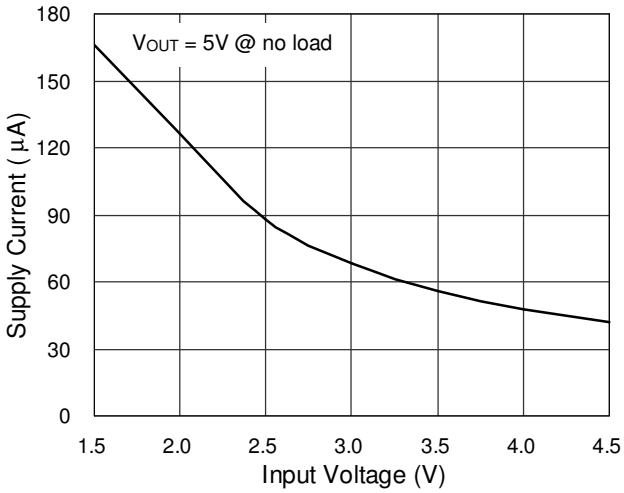
Input Current I(V_{DD}) vs. Output Current



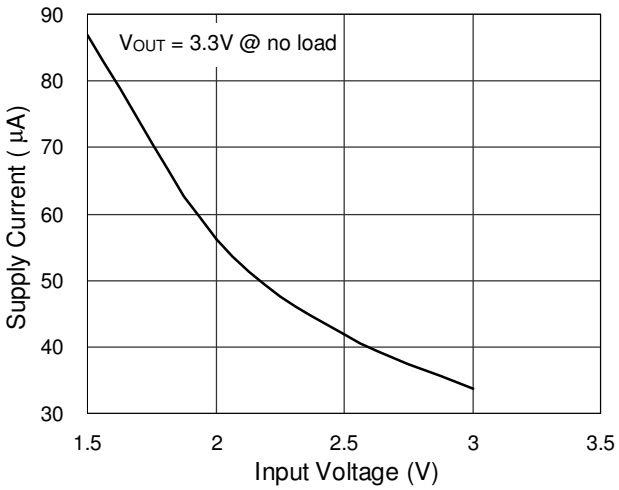
Input Current I(V_{DD}) vs. Input Voltage



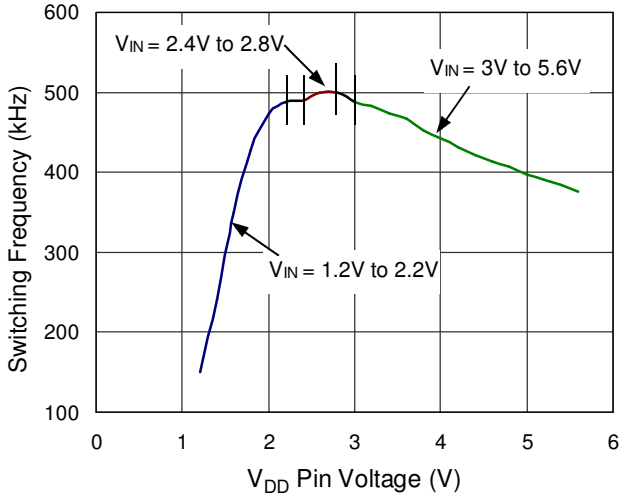
Supply Current I(V_{IN}) vs. Input Voltage



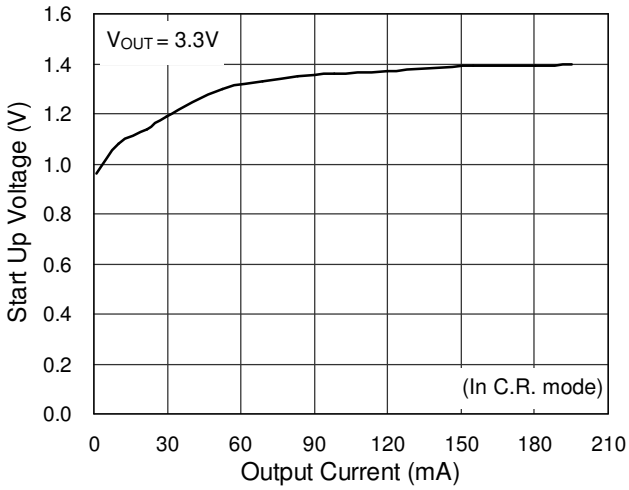
Supply Current I(V_{IN}) vs. Input Voltage



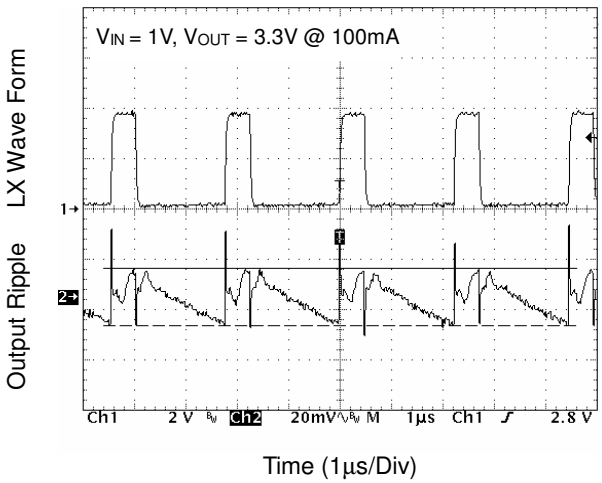
Switching Frequency vs. V_{DD} Pin Voltage



Start Up Voltage vs. Output Current

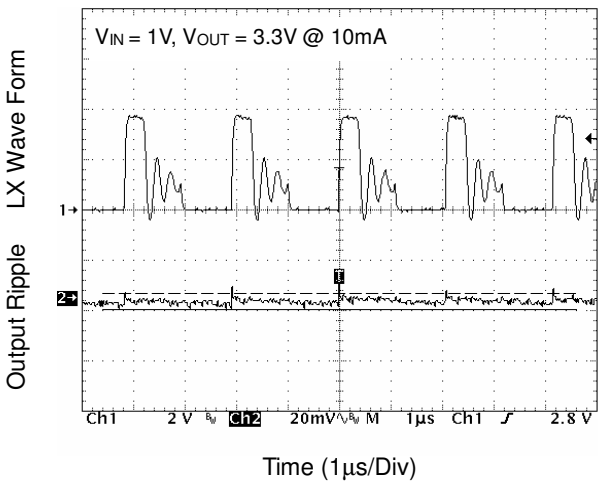


LX Pin Wave Form & Output Ripple



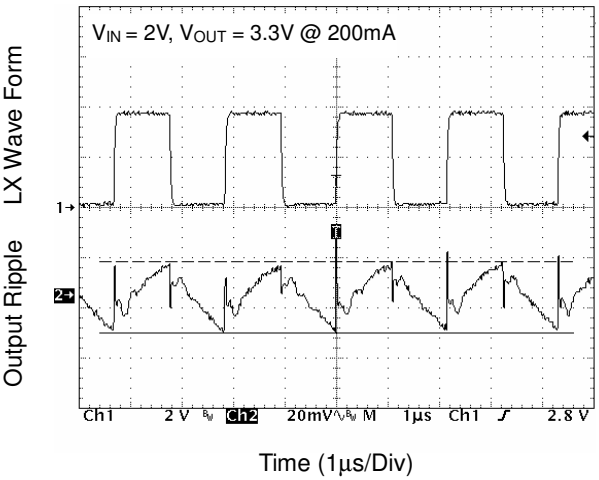
Time (1µs/Div)

LX Pin Wave Form & Output Ripple



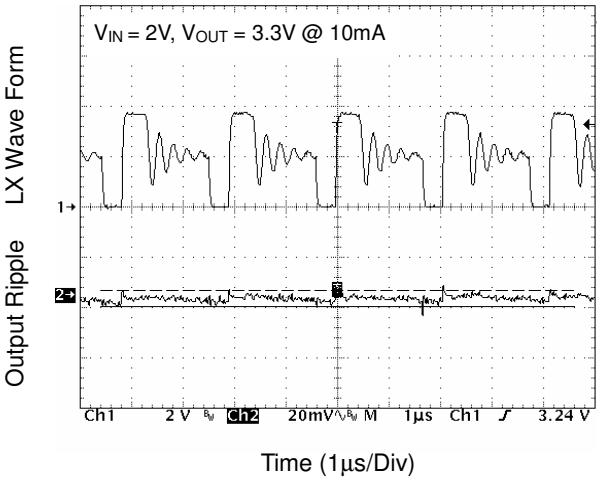
Time (1µs/Div)

LX Pin Wave Form & Output Ripple



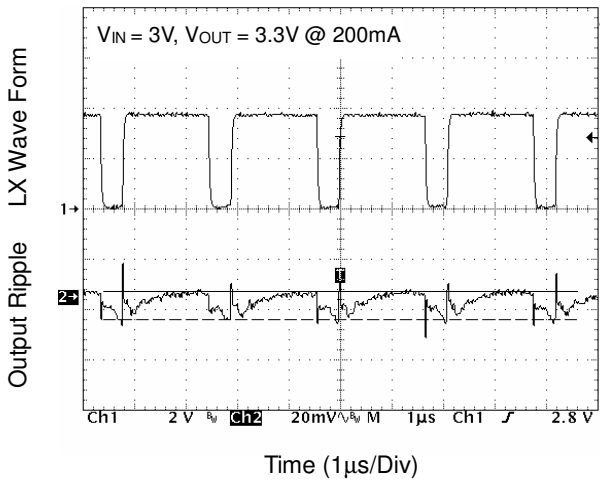
Time (1µs/Div)

LX Pin Wave Form & Output Ripple



Time (1µs/Div)

LX Pin Wave Form & Output Ripple



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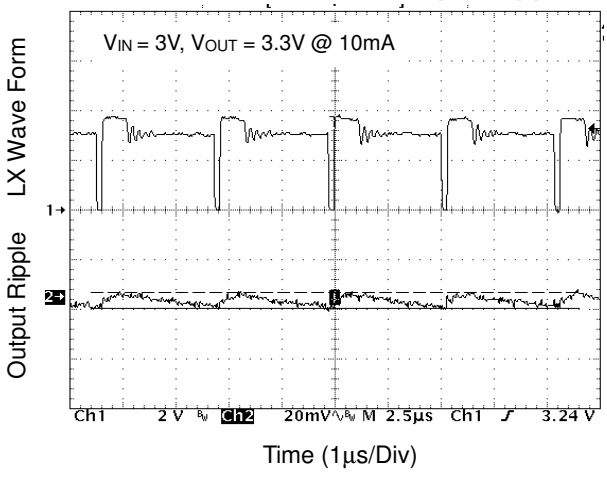
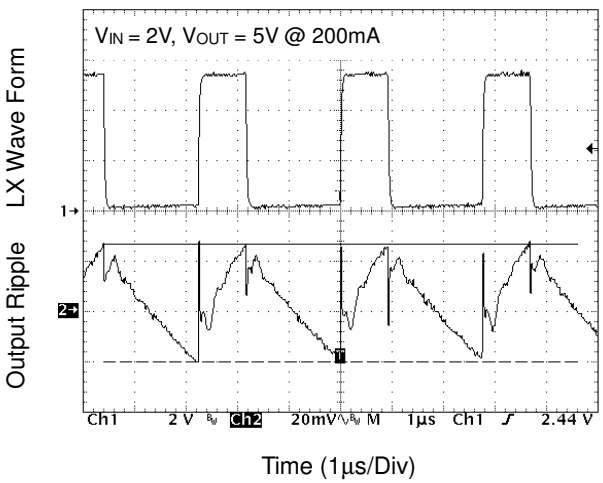
LX Pin Wave Form & Output Ripple



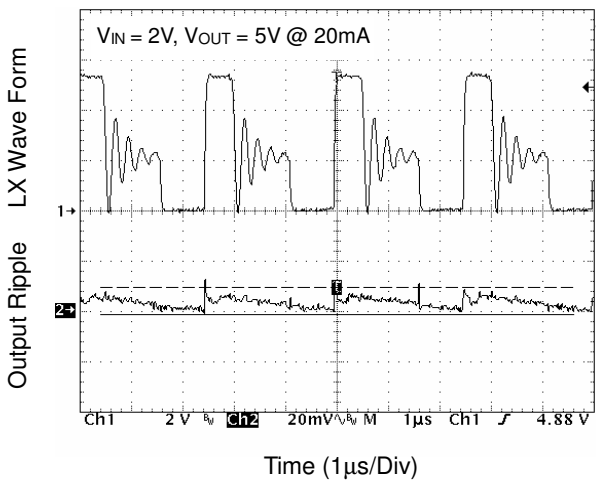
Time (1µs/Div)

LX Pin Wave Form & Output Ripple



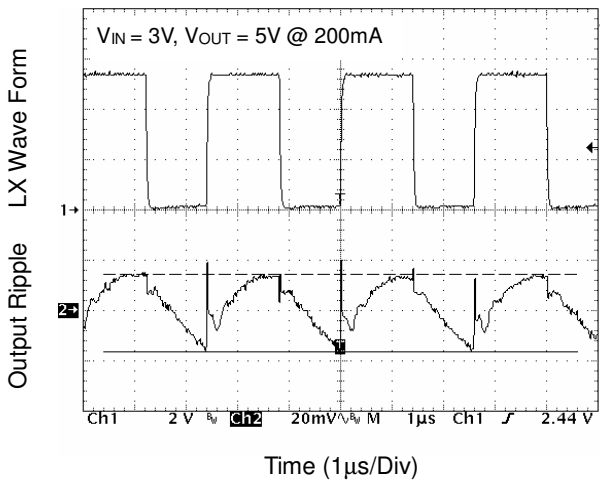
Time (1µs/Div)

LX Pin Wave Form & Output Ripple



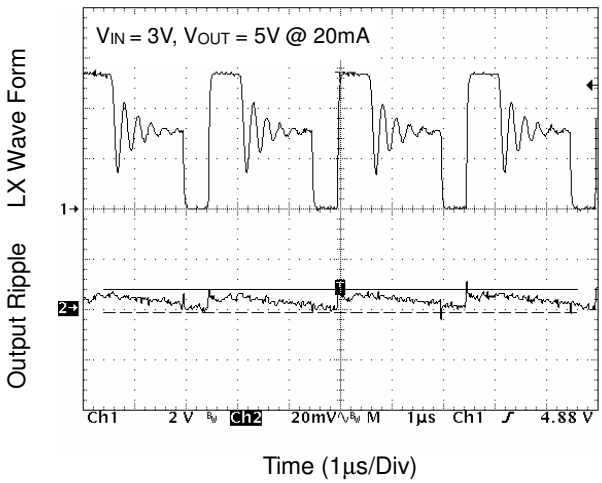
Time (1µs/Div)

LX Pin Wave Form & Output Ripple



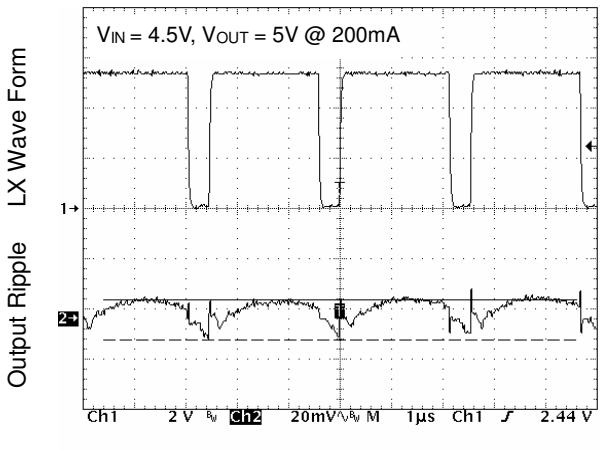
Time (1µs/Div)

LX Pin Wave Form & Output Ripple



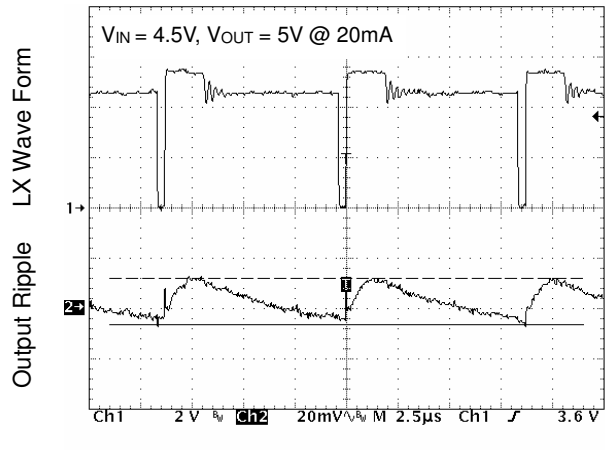
Time (1µs/Div)

LX Pin Wave Form & Output Ripple



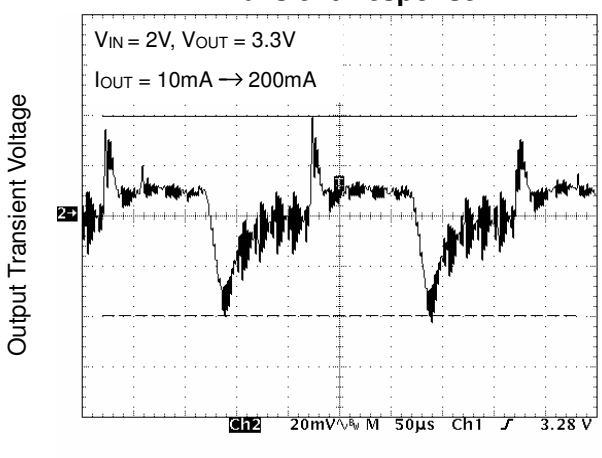
Time (1µs/Div)

LX Pin Wave Form & Output Ripple



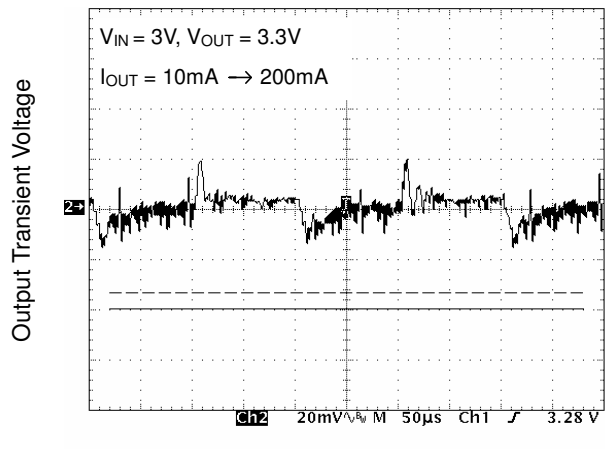
Time (1µs/Div)

Transient Response



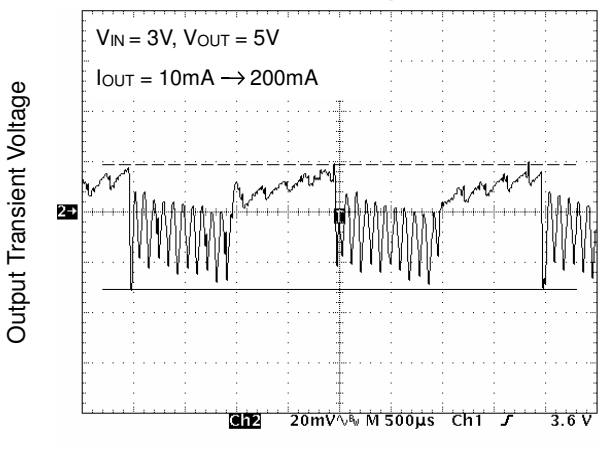
Time (50µs/Div)

Transient Response



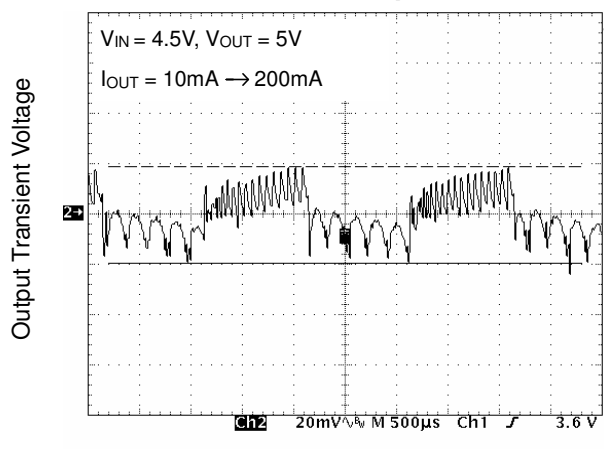
Time (50µs/Div)

Transient Response



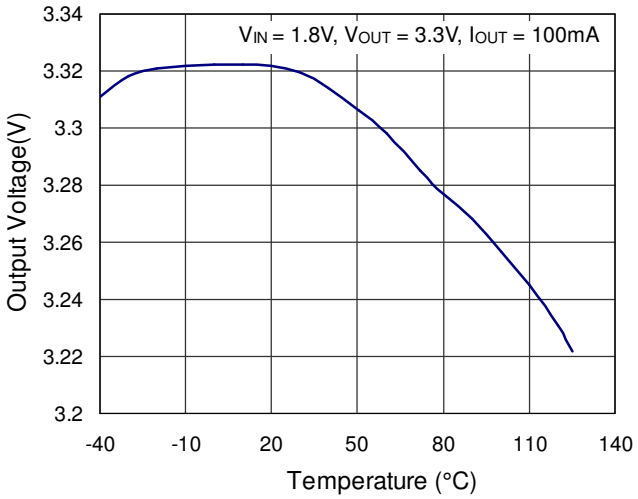
Time (50µs/Div)

Transient Response

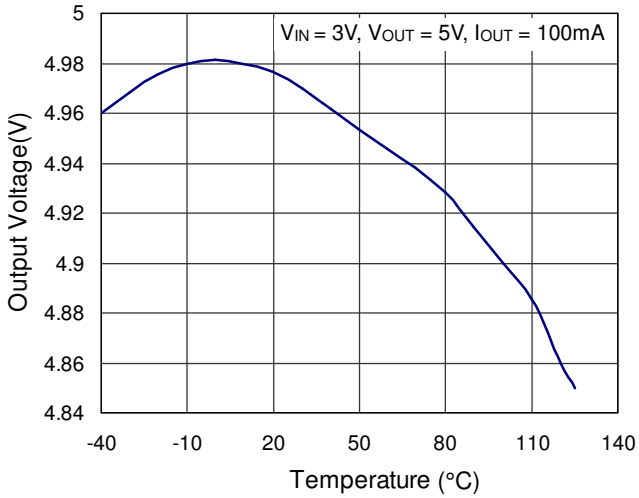


Time (50µs/Div)

Output Voltage vs. Temperature



Output Voltage vs. Temperature



Application Information

Output Voltage Setting

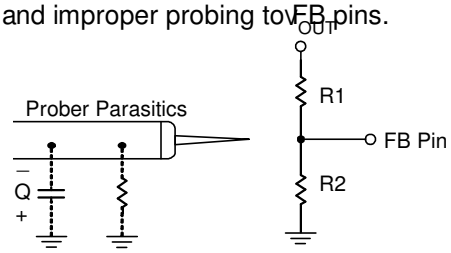
Referring to Typical Application Circuits, the output voltage of the switching regulator (V_{OUT}) can be set with Eq.1.

$$V_{OUT} = (1 + \frac{R1}{R2}) \times 1.25V \qquad \text{Eq.1}$$

Feedback Loop Design

Referring to Typical Application Circuits. The selection of R1 and R2 based on the trade-off between quiescent current consumption and interference immunity is stated below:

- Follow Eq.1
- Higher R reduces the quiescent current (Path current = 1.25V/R2), however resistors beyond 5MΩ are not recommended.
- Lower R gives better noise immunity, and is less sensitive to interference, layout parasitics, FB node leakage, and improper probing to FB pins.



- A proper value of feed forward capacitor parallel with R1 can improve the noise immunity of the feedback loops, especially in an improper layout. An empirical suggestion is around 0~33pF for feedback resistors of MΩ, and 10nF~0.1μF for feedback resistors of tens to hundreds KΩ.

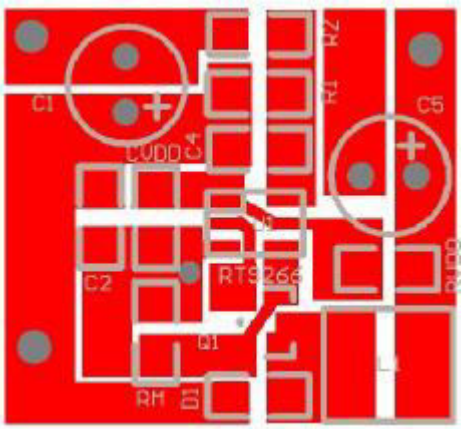
For applications without standby or suspend modes, lower values of R1 and R2 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1 and R2 are needed. Such "high impedance feedback loops" are sensitive to any interference, which require careful layout and avoid any interference, e.g. probing to FB pin.

Layout Guide

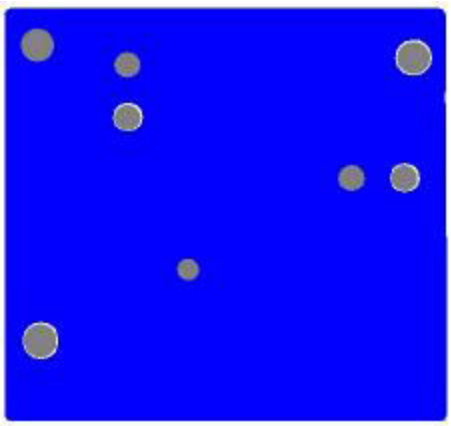
- A full GND plane without gap break.
- V_{DD} to GND noise bypass – Short and wide connection for the 1μF MLCC capacitor between Pin5 and Pin3.
- V_{IN} to GND noise bypass – Add a capacitor close to L1 inductor, when V_{IN} is not an idea voltage source.
- Minimized FB node copper area and keep far away from noise sources.
- Minimized parasitic capacitance connecting to LX and EXT nodes, which may cause additional switching loss.

Board Layout Example (2-Layer Board)

(Refer to Typical Application Circuits Figure 2 for the board)

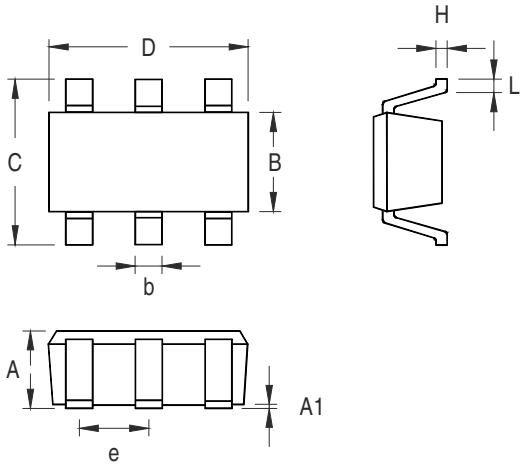


- Top Layer -



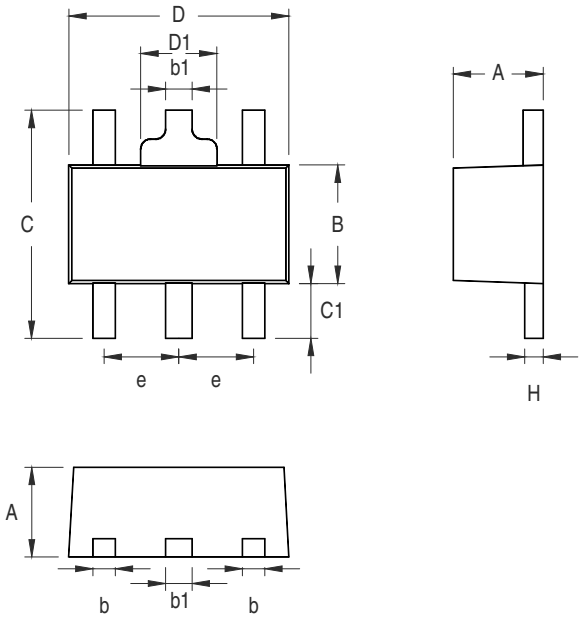
- Bottom Layer -

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.559	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT- 26 Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.360	0.520	0.014	0.020
B	2.400	2.600	0.094	0.102
b1	0.406	0.533	0.016	0.021
C	--	4.250	--	0.167
C1	0.800	--	0.031	--
D	4.400	4.600	0.173	0.181
D1	--	1.700	--	0.067
e	1.400	1.600	0.055	0.063
H	0.380	0.430	0.014	0.017

5-Lead SOT-89 Surface Mount Package